PATENT NO. 348017

HIGH SPEED MICROPROCESSOR DESIGN AND IMPLEMENTATION

APPLICATION NO. 3238/CHE/2010

APPLICANT

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ABSTRACT

Microprocessor design and implementation is disclosed. This invention relates to microprocessors, and more particularly to design and implementation of microprocessors. Existing microprocessors employ a number of clock cycles for the execution of the instructions and thus leading to slowing down speed of execution. The microprocessor disclosed herein increases the speed of execution by providing specific hardware modules in the ALU of the processor. Further, the hardware modules are provided with a pre-defined set of instructions for enabling the hardware modules to increase the speed of execution. The microprocessor employs 4 stage pipelining, parallel processing techniques to increase the execution speed

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CLAIM 1

A microprocessor (101) with increased execution speed, said microprocessor (101) comprising an arithmetic and logic unit (ALU) (201) provided with specific hardware circuits, said hardware circuits configured for decoding and executing a set of pre-defined instructions, the ALU (201) comprising a parity module (401) configured for computing parity of a data word by employing pre-defined instruction, wherein the parity module (401) is configured to compute the parity by XORing data bits; a N-bit shift module (402) configured for determining the number of shifts to be performed on the data word from the pre-defined instructions and shifting bits of the data word by the number specified in the pre-defined instructions; a zero-bit insertion module (403) configured for inserting a zero bit in a data word by employing a pre-defined instruction for the bit insertion; a memory block copy module (404) configured for transferring a block of data from a first memory location to a second memory location by employing a pre-defined instruction; and a N-bit Cyclic Redundancy Check (CRC) module (405, 406, 407, 408) configured for employing pre-defined instructions for computing the CRC of data in a transmitter system; a program memory module (208) configured for storing said pre-defined instructions; and sending said pre-defined instructions to said ALU (201) on obtaining a signal from a control unit (202); a data memory module (207) configured for storing data required for the execution of said pre-defined instructions; and providing said stored data to said ALU (201) during execution of said pre-defined instructions.